Claims

1. An arbiter for a system having multiple bus masters each having real time requirements for mastership of a bus, wherein the arbiter is arranged so that the amount of time that each bus master can gain bus access is a percentage of the total bus time.

2. An arbiter as claimed in claim 1, further comprising means for allocating priority levels for bus mastership when a given bus master does not request bus mastership during its allocated percentage of the total bus time.

3. A system having a bus, multiple bus masters each having real time requirements for mastership of the bus, and an arbiter for allocating bus mastership to the bus masters, wherein the arbiter is as claimed in claim 1 or claim 2.

4. A system as claimed in claim 3, wherein the system comprises a QMS, and each bus master is a queue user.

5. A QMS system as claimed in claim 4, wherein the QMS includes a queue portal for each of the queue users, a respective queue user interface being positioned between each queue user and its portal.

6. A QMS system as claimed in claim 4 or claim 5, further comprising a memory for holding data as it passes through the queues, and wherein one of the queue users is constituted by a processor.

7. A QMS system as claimed in any one of claims 4 to 6, wherein the arbiter includes a state machine for allocating each bus master its predetermined percentage of bus time.

8. A QMS system as claimed in claim 7 when appendant to claim 5, wherein the state machine determines the active queue portal arbitration by cycling through a

predetermined number of states, in a fixed order, or every clock cycle, each of the states being associated with a respective queue portal.

9. A QMS system as claimed in claim 8, wherein the percentage of total bus time allocated to a given queue portal is determined by the number of states associated with that queue portal.

10. A QMS system as claimed in any one of claims 5 to 9, wherein the means for allocating priority levels for bus mastership is activated when the queue portal currently selected does not request bus mastership.

11. A QMS system as claimed in claim 10 when appendant to claim 6, wherein the arbiter is such that the highest of said priority levels is allocated to non-interruptible memory sequences triggered by the processor.

12. A QMS system as claimed in claim 11, wherein the arbiter is such that the next highest priority level is allocated to accesses to the bus by the processor.

13. A QMS system as claimed in claim 13, wherein the arbiter is such that the next highest priority level is allocated to accesses to the bus by the QMS.

14. A Bluetooth baseband peripheral comprising a QMS system, link control hardware for communication with Bluetooth devices via a radio IC and the QMS system, and a re-usable microprocessor block, wherein the QMS system is as claimed in any one of claims 5 to 13.

15. A peripheral as claimed in claim 14, further comprising an interface block between the bus and the re-usable microprocessor block.

16. A peripheral as claimed in claim 14 or claim 15, wherein the queue users are a communication control block, a host queue user, a voice encoder and decoder, and a processor forming part of the re-usable microprocessor block.

17. A peripheral as claimed in any one of claims 14 to 16, wherein each of the queue users is connected to the bus via its queue user interface and a respective bus master and bus tri-state driver.